01-07-00

TRANSMITTAL LETTER
FOR FILING PATENT APPLICATION SPECIFICATION AND DRAWING
TO OBTAIN FILING DATE

Box Applications
Assistant Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Transmitted herewith for filing is the patent application of:

Inventor:	SIMON J. BROADLEY
Filed:	Concurrently herewith
Serial No.	
For:	SELF-OSCILLATING VARIABLE FREQUENCY CLASS D AMPLIFIER
Attorney Docket No.:	995-P-3

Enclosed are:

(1)	Specification (16 pages including title page; claims & abstract)
(2)	THREE (3) sheets of INFORMAL Drawings (Figs. 1-3)
(3)	Declaration, Petition and Power of Attorney
(4)	Declaration Verifying Small Entity Status
(5)	Other: _____

The filing fee has been calculated as shown below:

BASIC FEE	FILED	EXTRA FEE	**LARGE** ENTITY
$380.00			$ 380.00
Total Claims	1	0	$ 0.00
Indep. Claims	1	0	$ 0.00
TOTAL:			$ 380.00

Pursuant to the provisions of 37 C.F.R.§§ 1.10 and 1.53, applicant respectfully requests that this application be assigned a serial number and a filing dated of January 6, 2000, the date upon which the application was mailed to the U. S. Patent and Trademark Office by Express Mail No. EJ 742 156 507US

Respectfully submitted,

01/06/00
Date

TOD R. NISSLE, Reg. No. 29,241
TOD R. NISSLE, P.C.
P.O. Box 55630
Phoenix, Arizona 85078
Tel: 480-970-8700
Fax: 480-970-8707
Email: nissle@nissle.com

EXPRESS MAIL CERTIFICATION ACCOMPANYING PAPER AND/OR FEE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	SIMON J. BROADLEY
Filed:	Concurrently herewith
Serial No.	
For:	SELF OSCILLATING VARIABLE FREQUENCY CLASS D AMPLIFIER
Attorney Docket No.	995-P-3

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"EXPRESS MAIL" mailing label number: EJ 742 156 507US ✓

Date of Deposit: January 6, 2000

I hereby certify that the attached

Patent Application [16 pages including title page, specification, claims and abstract]; Three (3) Sheet[s] of Informal Drawings [Figs. 1-3]; Transmittal letter; and return postcard; are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to "Box Patent Applications, Assistant Commissioner for Patents, Washington, D.C. 20231."

TOD R. NISSLE, Reg. No. 29,241

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	**SIMON J. BROADLEY**
Serial No.	:	
Filed	:	**Concurrently herewith**
For	:	**SELF OSCILLATING VARIABLE FREQUENCY CLASS D AMPLIFIER**

DECLARATION VERIFYING SMALL ENTITY STATUS UNDER 27 C.F.R. 19(f) AND 1.27(b)

Asst. Commissioner of Patents,
Washington, D.C. 20231

Dear Sir:

As a named inventor, I hereby state that I qualify as an independent inventor as defined in 37 C.F.R. 1.9 (c) for purposes of paying reduced fees under § 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the above-identified patent.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license any rights the invention to any person who could not be classified as an independent inventor under 27 C.F.R. 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 C.F.R. 1.9(d) or a nonprofit organization under 37 C.F.R. 1.9 (e). Any person, concern or organization to which I have assigned, granted, conveyed or licensed or am under an obligation under contract or law to assign, grant, convey or license any rights in the invention is identified below:

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01-06-00

TOD R. NISSLE, Reg. No. 29,241 DATE

Full Name: N/A

Address: _____

_____

[ ] **Individual** [ ] **Small Business** [ ] **Non profit Organization**

Full Name: N/A

Address: _____

_____

[ ] **Individual** [ ] **Small Business** [ ] **Non profit Organization**

I acknowledge the duty to file, in this patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. [37 C.F.R. 1.28(b)]

I hereby declare that all statements herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements or the like so made are punishable by fine or imprisonment, or both, under §1001 to Title 18 of the United States Code, and that such willful false statement may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Inventor: SIMON J. BROADLEY

Address: 2265 East Stephens Road

Gilbert, Arizona 85296

Signature: [signature]

Date: 01-06-00

Name of Inventor: N/A

Address:

Signature:

Date:

Attorney's Docket No.: 995-P-3

SELF-OSCILLATING VARIABLE FREQUENCY CLOSED LOOP CLASS D AMPLIFIER

By

Simon J. Broadley

of

Gilbert, Arizona

A Citizen of Australia

I hereby certify that this correspondence is being deposited with the United States Postal Service as U.S. Express Mail EJ 742 156 507 US in an envelope addressed to: COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231 on January 6, 1999.

January 6, 1999

TOD R. NISSLE, Reg. No. 29,241 DATE

SELF OSCILLATING VARIABLE FREQUENCY CLOSED LOOP CLASS D AMPLIFIER

This invention pertains to amplifiers.

More particularly, the invention pertains to an improved Class D amplifier which does not utilize a clock, which is self-oscillating, and which reduces switching errors and distortions.

Conventional Class D amplifiers are each comprised of an integrator summed with a fixed frequency triangle wave and inputted into the switch control. The switching waveform is filtered through a Low Pass Filter (LPF) and outputted to the speaker or other load. Such amplifiers are illustrated in Figs. 1 to 3 of U.S. Patent Number 4,415,863, and have certain disadvantages.

First, the clock frequency in the amplifiers is fixed, resulting in a constant, large, high frequency component that can potentially create noise in

FM tuners, switching power supplies, or other parts of an audio system.

Second, the clock frequency is generally selected to optimize operation under heavy load conditions. As a result, when an audio signal input is not applied, poor signal to noise ratio measurements are produced.

Third, the feedback is such prior art systems is taken prior to the low pass filter. This makes it difficult to control the speaker because a nonlinear generation of the sine wave is produced as the load of the speaker changes impedance. This causes poor total harmonic distortion and poor noise and damping factor measurements.

Accordingly, it would be highly desirable to provide an improved Class D amplifier which would compensate for problems caused by a fixed clock frequency and which would yield better speaker control.

Therefore, it is a principal object of the invention to provide an improved Class D amplifier.

A further object of the instant invention is to provide an improved Class D amplifier which reduces the likelihood that excess noise will be created in remaining portions of an audio system used in combination with the Class D amplifier.

Another object of the invention is to provide an improved Class D

amplifier which enables better control of a speaker receiving an analog signal from the amplifier.

These and other, further and more specific objects and advantages of the invention will be apparent to those skilled in the art from the following detailed description thereof, taken in conjunction with the drawings, in which:

Fig. 1 is a block diagram illustrating a Class D amplifier constructed in accordance with the principles of the invention;

Fig. 2 is a circuit diagram illustrating the amplifier of Fig. 1; and,

Fig. 3 is a Spice diagram illustrating the analog signal produced by the Class D amplifier superimposed on the square wave generated in the amplifier prior to production of the analog signal.

Briefly, in accordance with the invention, I provide an improved self-oscillating audio Class D amplifier for an input signal. The amplifier includes a detector for receiving a control signal and producing a digital waveform switching signal to activate one of a pair including a positive switch and a negative switch to correct gain produced by the Class D amplifier; an output stage including a positive switch and a negative switch, the output stage receiving the switching signal and activating one of the switches to produce a digital driving signal; an output filter to receive the digital driving signal,

remove switching noise and provide an amplified audio analog output signal to drive a load; and, an error detection amplifier circuit to receive the amplified analog output signal and compare the output signal to the input audio signal for gain-correction purposes, and to produce the control signal.

Turning now to the drawings, which depict the presently preferred embodiments of the invention for the purpose of illustrating the practice thereof and not by way of limitation of the scope of the invention, and in which like reference characters refer to corresponding elements throughout the several views, Fig. 1 illustrates a Class D amplifier constructed in accordance with the principles of the invention and including error amplifier circuit 14, zero cross detector 15, output stage 16, output filter 19, feedback signal 21, and speaker 20 or another load. Circuit 14 produces an ADJ OUT control signal 17. Detector 15 produces a DIG OUT signal 18.

In the circuit diagram of Fig. 2, the error amplifier circuit 14 includes resistors R1, R2, R3 and amplifier A. The zero crossing detector 15 includes VCC +20V, includes resistors R4, R5, includes current source C2, and includes transistors T1, and T2. The output stage 16 includes MOSFET switches M1 and M2, the driver circuitry MC1 for MOSFET switch M1, the driver circuitry MC2 for MOSFET switch M2, power supply VCC, power

supply VEE, transistors T3 and T4, current source C1, and resistors R6 and R7. The output filter 19 includes inductor L, capacitor C, and AMP OUT.

In operation, an audio analog input signal 12 is fed into an error amplifier circuit 14 that adjusts the signal and produces a digital ADJ OUT signal 17. The ADJ OUT control signal 17 is a step response PWM waveform.

The signal ADJ OUT control 17 is received by zero crossing detector 15 and transformed into a high frequency digital DIG OUT signal 18. In this respect, zero crossing detector 15 functions as a pulse width modulator.

The zero crossing detector 15 also separates out positive and negative signals and determines whether the high side MOSFET switch M1 is turned on or whether the low side MOSFET switch M2 is turned on. MOSFET switch M1 is connected to the positive rail. MOSFET switch M2 is connected to the negative rail. Consequently, if the voltage is positive, detector 15 turns on the high side positive switch M1. If the voltage is negative, detector 15 turns on the low side negative switch M2. While the circuit is operating, switches M1 and M2 toggle back and forth continuously. Zero crossing detector 15 alternates between the M1 and M2 switches but does not allow both switches to be on at the same time.

The output of the zero crossing detector 15 controls the switches

M1 and M2 in the output stage 16.

The high frequency digital signal (DGI OUT) 18 is received by the output stage 16. When signal 18 activates positive switch M1, switch M1 is connected to summing point S and is pulled up to VCC. When signal 18 activates negative switch M2, switch M2 is connected to summing point S and is pulled down to VEE. VCC is a positive power supply which produces, by way of example and not limitation, 50 volts to 100 volts. VEE is a negative power supply which produces, by way of example and not limitation, minus 50 to minus 100 volts.

The analog signal coming out of the output filter 19 is a sine wave 32. In Fig. 3 sine wave 32 is superimposed on the switching square wave 33. Square wave 33 represents the switching between MOSFET switches M1 and M2. The width of a pulse in square wave 33 is the length of the horizontal portion at the top or bottom of the pulse. Consequently, the width of the pulse when sine wave 32 output is at about 50V (as indicated by point 34) is, in Fig. 3, much longer than the width of the pulse when the sine wave output is at about 0 V (as indicated by point 35).

The signal from the output stage 16 is received by the output filter 19.

The output filter 19 removes high frequency components (include switching noise) having frequencies in the range of about 10 KiloHertz to 250 KiloHertz. The resulting low frequency sine wave signal which leaves filter 19 typically has a frequency in the range of about 20 Hertz to 200 Hertz. Filter 19 also converts the digital signal from stage 16 back into an analog signal capable of driving an external load like speaker 20. The output signal from filter 19 is an amplified version of the audio input signal. The output signal from filter 19 typically has a gain in the range of five to fifteen, although the gain can vary as desired.

Feedback 21 is taken from the signal produced by output filter 19. The feedback 21 is returned to a difference amplifier in the error amplifier circuit 14. The difference amplifier compares the amplitudes and phase relationships of the feedback 21 and of the audio in signal 12. Resistors R1 and R2 function to compensate for the gain in the feedback signal such that the feedback signal is divided down by resistors R1 and R2 and then passes into the difference amplifier, and such that the divided down feedback signal has an amplitude and phase which ideally is identical to the amplitude and phase of the audio in signal 12.

If the amplitude of the divided down feedback signal is not

equivalent to that of the audio in signal, then the error amplifier circuit 14 sends a counter pulse or control signal 17 to compensate. For example, if the feedback signal 21 (after being divided down by resistors R1 and R2) indicates that the positive voltage is too low (i.e., the gain with respect to the audio signal 12 input to circuit 14 is 9.9 to 1.0 instead of a desired 10.0 to 1.0, or, in other words the voltage output from output filter 19 for a point along sine wave 32 is not as great as desired) then the counter pulse from circuit 14 activates transistors T1 and T4 to hold switch M1 on or closed until the feedback signal indicates that the gain is at least 10.0 (or greater than 10.0) to 1.0.

If the feedback signal 21 (after being divided down by resistors R1 and R2) indicates that the positive voltage is too high (i.e., the gain with respect to the audio signal 12 input to circuit 14 is 10.1 to 1.0 instead of a desired 10.0 to 1.0, or, in other words the voltage output from output filter 19 for a point along sine wave 32 is greater than desired) then the counter pulse from circuit 14 activates transistors T2 and T3 to hold switch M2 on or closed until the feedback signal indicates that the gain is at least 10.0 (or less than 10.0) to 1.0.

If the feedback signal 21 indicates that the negative voltage is too high (i.e., the gain is 10.1 to 1.0 instead of 10.0 to 1.0), then the counter pulse

from circuit 14 activates transistors T1 and T4 to hold switch M1 on or closed until the feedback signal indicates that the gain is 10.0 (or less than 10.0) to 1.0.

If the feedback signal 21 indicates that the negative voltage is too low (i.e., the gain is 9.8 to 1.0 instead of 10.0 to 1.0), then the counter pulse from circuit 14 activates transistors T2 and T3 to hold switch M2 on or closed until the feedback signal indicates that the gain is 10.0 (or greater than 10.0) to 1.0.

If the error is small, i.e. if the gain is 10.0 or is close to 10.0, then width of pulses in the square wave signal 33 leaving the output stage 16 is small and the pulses leave stage 16 at a higher frequency.

If the error is large, i.e. if the gain is not close to 10.0 (but is, for example 10.3), then the width of pulses in the square wave signal 33 leaving the output stage 16 is larger and the pulses leave stage 16 at a lower frequency.

By way of further example, if after comparing the feedback signal 21 to the input signal 12, the error amplifier circuit 14 determines that at point 31 on the sine wave 32 the voltage is 50 volts instead of the desired 51 volts, circuit 14 compensates by turning on switch M1 until the voltage on sine wave 32 increases to a desired level.

By way of further example, if after comparing the feedback signal 21 to the input signal 12, the error amplifier circuit 14 determines that at point 30 on the sine wave 32 the voltage is at minus 41 volts instead of the desired minus 39 volts, the circuit 14 compensates by turning on switch M1 until the voltage on sine wave 32 "decreases" from minus 41 volts to the desired minus 39 volts.

By way of further example, if power supply VCC produces 100 volts, if the signal produced by filter 19 is producing positive voltage with a gain of nine with respect to input signal 12, and if a gain of ten is desired, then circuit 14 produces a positive signal to turn on switch M1 until the gain increases to ten. If the gain happens to increase past ten to, for example, 10.1, then circuit 14 produces a negative signal to turn on switch M2 until the gain for the positive voltage decreases back to ten. This automatic "self oscillating" or "hunting"pattern eventually typically results in there only being a small error between the actual gain in the signal leaving filter 19

A classic Class D amplifier has a built in clock and constantly switches.

One primary advantage of the Class D amplifier of the invention is that it does not utilize or require a clock and does not require the additional

parts necessary to produce a clock signal.

As would be appreciated by those of skill in the art, constant currents sources C1 and C2 constantly deliver current for the availability of other electronic components.

When it is desired to turn on MOSFET switch M1, error amplifier circuit 14 produces a positive signal which turns on transistor T1 and pulls current through resistor R4 and transistor T4 resutling in current sourced to resistor R6 generating a voltage for the buffer MC1.

When it is desired to turn on MOSFET switch M2, error amplifier circuit 14 produces a negative signal which turns on transistor T2 and pulls current through resistor R5 and transistor T3 resulting in current sourced to resistor R7 generating a voltage for the buffer MC2.

A buffer or any other desired circuitry can be utilized in MC1 and MC2 to drive switches M1 and M2. If desired a transistor, IGBL or other switch can be utilized in place of switches M1 and M2. A transformer or other switch activation means can be utilized in place of transistors T1 to T4.

Filter 19 can be a two pole filter, four pole filter, six pole filter, or any other filter means which performs the function of removing high frequencies and producing an analog signal for a speaker or other load.

As the magnitude of the error between the desired gain produced by the amplifier of the invention increases, operation of the amplifier circuit slows. In particular, when a switch M1, M2 is held open to compensate for an error, current ramps up through inductor L, voltage ramps up through capacitor C, and voltage ramps up at the AMP OUT intermediate the inductor L and capacitor C. The time required to ramp up current or voltage, as the case may be, slows operation of the circuit and facilitates large error corrections. Slowing down the operation of the circuit also improves the efficiency of the circuit by not forcing the circuit to continually switch, which generates additional switching losses.

When switching is occurring and is producing the square wave pattern shown in Fig. 3, the amplifier circuit of the invention allows the output stage 16 to latch to the power supply rail, reducing the frequency of operation so that it equals the frequency of operation of the input. Such latching minimizes switching dissipation and maximizes the possible output of the system.

When the magnitude of the error between the desired gain and gain actually produced in the signal exiting filter 19 is at a minimum, the frequency of switching increases and the width of each pulse decreases due to

the minimal amount of correction necessary to maintain proper output. This "speeding up" helps maintain low noise performance when little or no signal is applied. This increase in noise performance is a by-product of the increased switching speed being filtered more efficiently by the output filter.

Having described my invention in such terms as to enable those of skill in the art to make and practice it, and having described the presently preferred embodiments thereof, I Claim:

Claims

1. A self oscillating audio Class D amplifier, comprising

(a) a detector for receiving a control signal and producing a digital waveform switching signal to activate one of a pair including a positive switch and a negative switch to correct gain produced by the Class D amplifier;

(b) an output stage including a positive switch and a negative switch, said output stage receiving said switching signal and activating one of said switches to produce a digital driving signal;

(c) an output filter to receive said digital driving signal, remove switching noise and provide an amplified audio analog output signal to drive a load;

(d) an error amplifier circuit to

(i) receive said amplified analog output signal and compare said output signal to said input audio signal for gain-correction purposes, and

(ii) produce said control signal.

ABSTRACT OF THE DISCLOSURE

An improved Class D amplifier which does not utilize a clock, is self-oscillating, and reduces switching errors and distortions. The amplifier includes positive and negative switches which are selectively activated to reduce errors in gain in the analog signal produced by the amplifier.

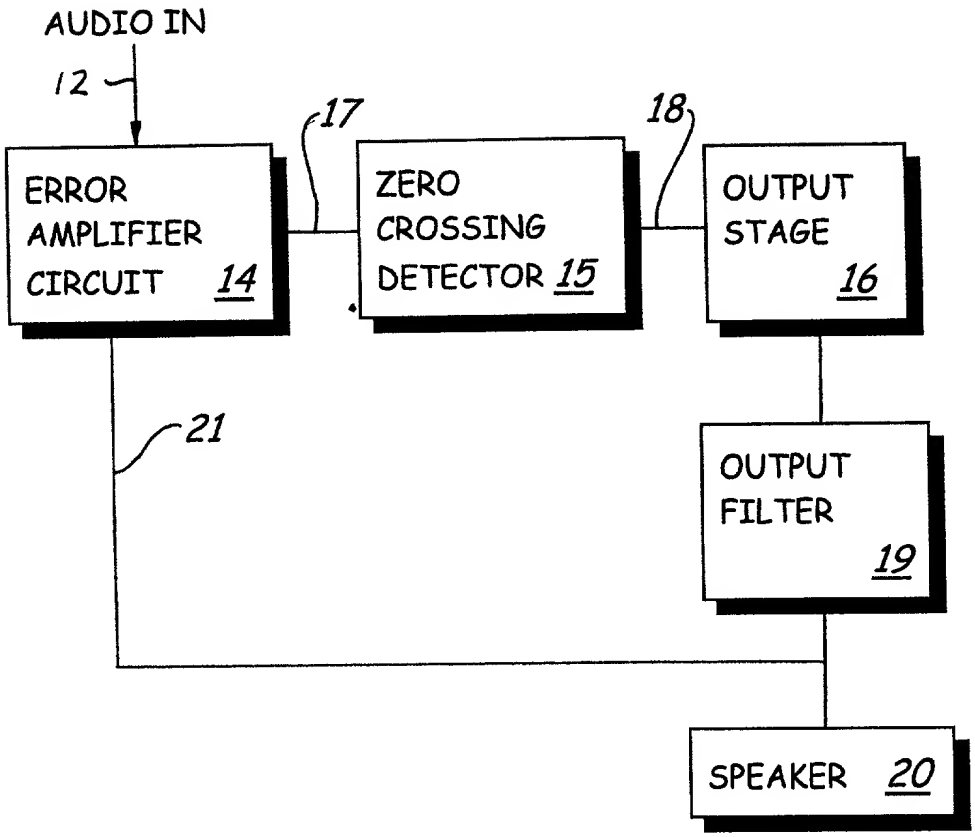
AUDIO IN
12
17
18
ERROR AMPLIFIER CIRCUIT 14
ZERO CROSSING DETECTOR 15
OUTPUT STAGE 16
21
OUTPUT FILTER 19
SPEAKER 20

FIG. 1

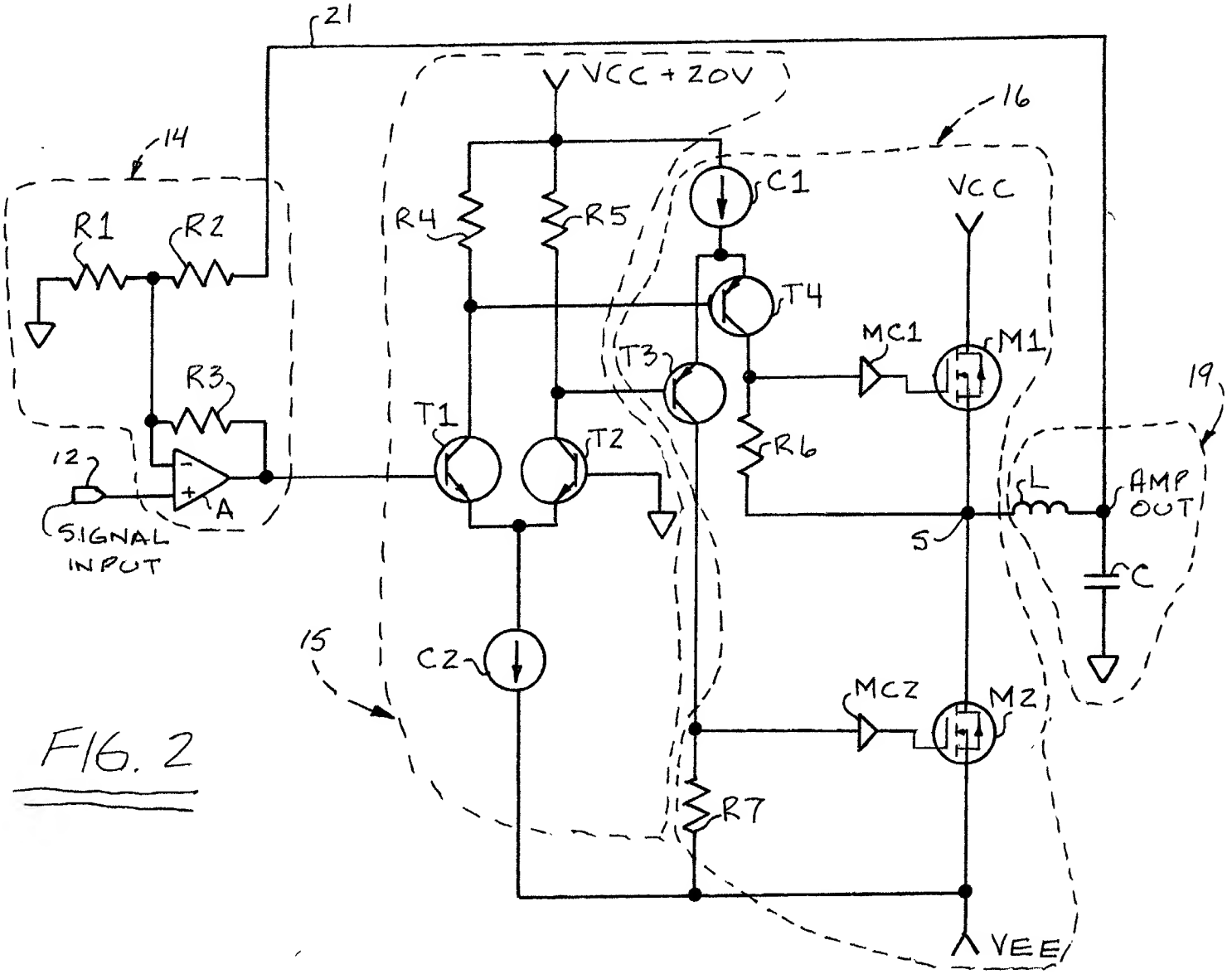

FIG. 2

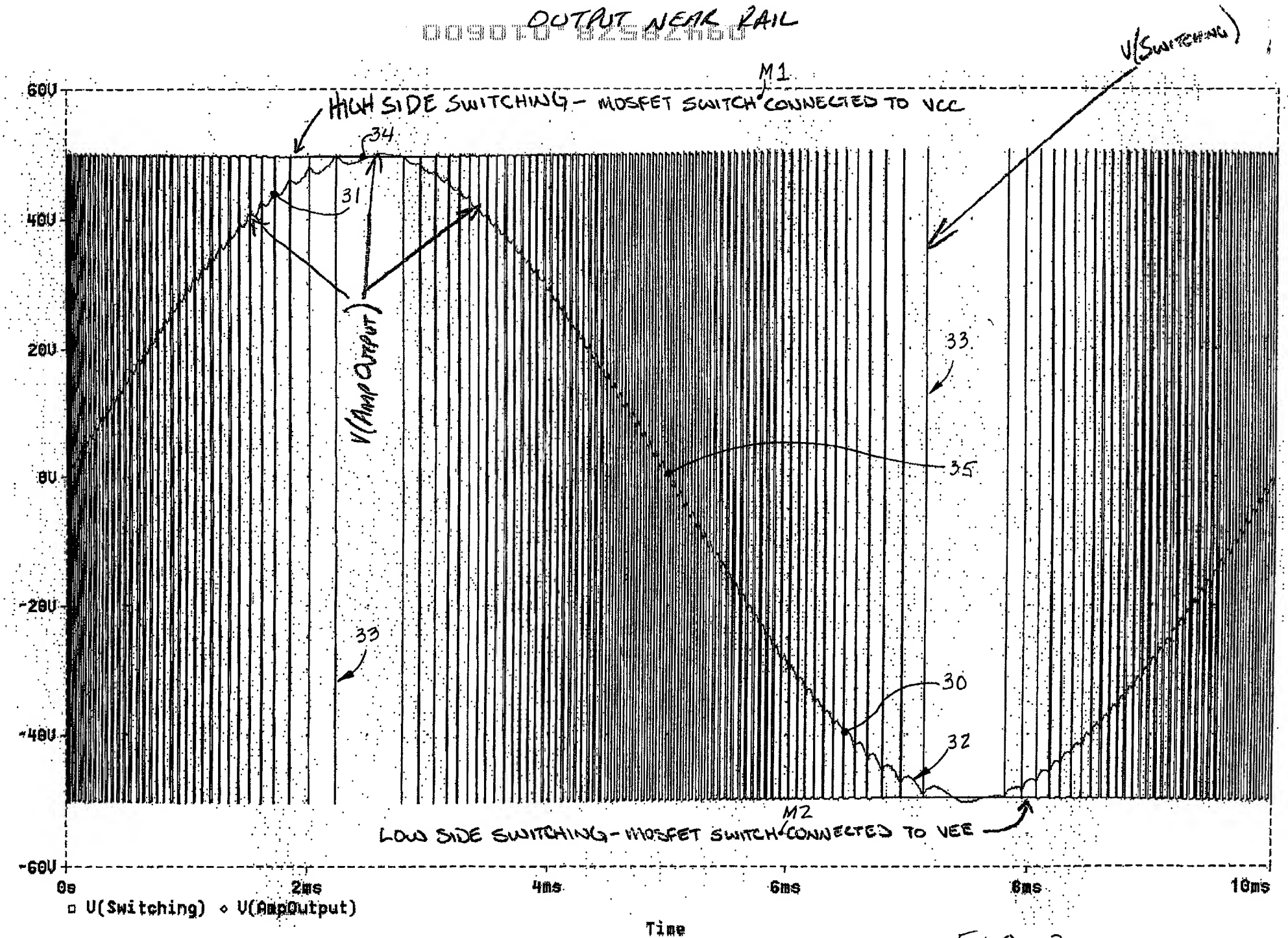

FIG. 3

DECLARATION, POWER OF ATTORNEY, AND PETITION

As a below named inventor, I hereby declare that:

My residence, post office address and citizen ship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SELF OSCILLATING VARIABLE FREQUENCY CLOSED LOOP CLASS D AMPLIFIER the specification of which:

(check one) xx is attached hereto. _____ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code §§ 119; 365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which the priority is claimed:

Prior Foreign Application(s)

			Priority Claimed	
N/A				
(Number)	(Country)	Day/month/year filed	Yes	No
N/A				
(Number)	(Country)	Day/month/year filed	Yes	No
N/A				
(Number)	(Country)	Day/month/year filed	Yes	No

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01-06-00

TOD R. NISSLE, Reg. No. 29,241 DATE

I hereby claim the benefit under Title 35, United States Codes §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations §156(a) which occurred between the filing date of the prior application and the national or PCT international filing of this application:

N/A
(Application Serial No) (Filing Date) (Status) (patented, pending, abandoned)

N/A
(Application Serial No) (Filing Date) (Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint:

Tod R. Nissle, Esq. Reg. No. 29,241
TOD R. NISSLE, P.C.
P.O. Box 55630
Phoenix, Arizona 85078

Tel: (480) 970-8700
Fax: (480) 970-8707
Email: nissle@nissle.com

my attorney and will full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith.

Wherefor I pray that Letters Patent be

granted to me for the invention or discover described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, this petition.

Full name of sole or first inventor: SIMON J. BROADLEY

Inventor's signature: _____ Date: 01-06-00

Residence: 2265 East Stephens Road, Gilbert, Arizona 85296

Citizenship: AUSTRALIA

Post Office Address: Same

Full name of second inventor: N/A

Inventor's signature: _____ Date: _____

Residence: _____

Citizenship: _____

Post Office Address: _____

(Supply similar information and signature for third and subsequent joint inventors)

Attorneys Docket No.: 995-P-3